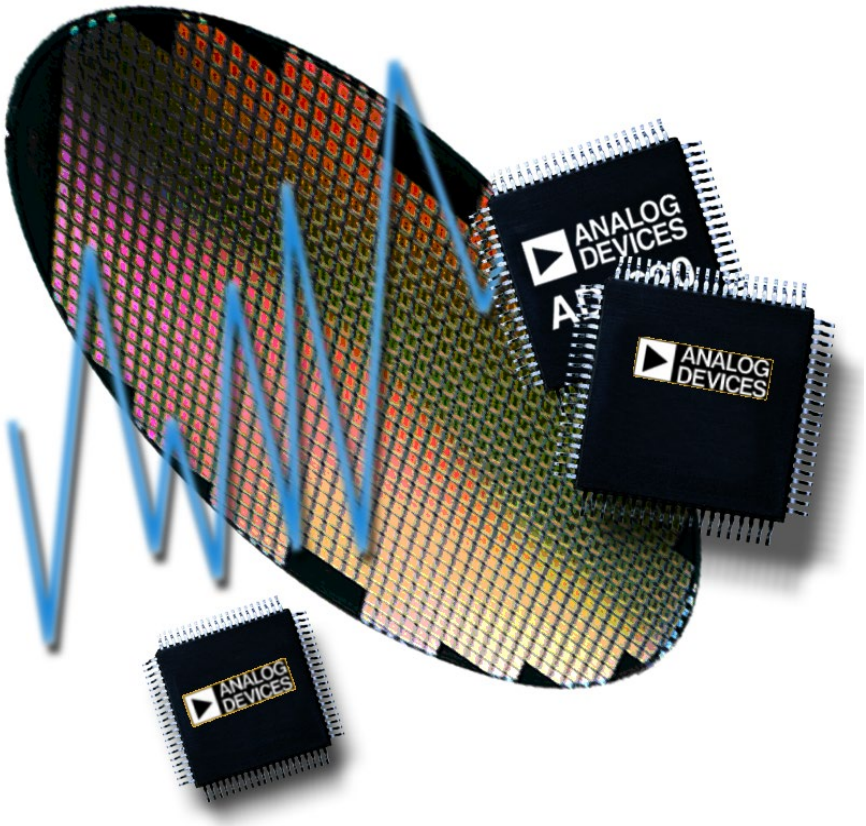

Reliability Report

Report Title: ADAU1850 Die Revison Qualification

Report Number: 19072

Revision: A

Date: 6 January 2022

Summary

This report documents successful completion of the reliability qualification requirements for the release of the ADAU1850 product in a 28-WLCSP package. The ADAU1850 is a three ADC, one DC, low-power codec with audio/fast DSPs. This die revision was performed to (1) to improve performance in single input mode and (2) to be applicable to case without external 24.576MHz as system clock.

Table 1: ADAU1850 Product Characteristics

Die/Fab

Die Id	TMPV51/A
Die Size (mm)	2.997 x 1.797
Wafer Fabrication Site	TSMC-Fab 14
Wafer Fabrication Process	40nm CMOS
Approximate Transistor Count	10,000
Passivation Layer	undoped-oxide/SiN
Bond Pad Metal Composition	AlCu

Package/Assembly

Package	28-WLCSP
Bump Pitch (mm)	0.4
Bump Diameter (mm)	0.24
Bumping Foundry	TSMC-Fab 14
RDL Composition	Ti(0.05)/Cu(0.3)/Cu(4)
RDL Repassivation	Layer 1: PBO (7.5) Layer 2: PBO (7.5)
Under Bump Metallization	Ti(0.05)/Cu(0.3)/Cu(8.6)
Bumping Process	Cu RDL Bump
Bump Composition	95.5Sn_4.0Ag_0.5Cu
Moisture Sensitivity Level	1
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 through 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: WLCSP at TSMC Fab-14 Package Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADAU1860	Q17772.1.HS1	45	0
Temperature Cycling (TC)	JESD22-A104	-40°C/125°C, Soak3, 10-14°C/min, 1,000 Cycles	ADAU1860	Q17772.1.TC1	45	0
				Q17772.2.TC2	45	0
				Q17772.3.TC3	45	0
				Q18938.1.TC1	45	0
			ADAU1850	Q17771.1.TC1	45	0
				Q17771.2.TC2	45	0
				Q17771.3.TC3	45	0
Unbiased HAST (UHST)	JESD22-A118	130°C 85%RH 33.3 psia, 96 Hours	ADAU1860	Q17772.1.UH1	45	0
				Q17772.2.UH2	45	0
				Q17772.3.UH3	45	0
				Q18938.1.UH1	77	0
			ADAU1850	Q17771.1.UH1	45	0
				Q17771.2.UH2	45	0
				Q17771.3.UH3	45	0
Temperature Humidity Bias (THB)	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAU1787	Q13146.5	45	0
				Q13146.6	45	0
				Q13146.7	45	0
				Q15092.15	45	0
				Q15093.8	45	0
				Q16587.8	45	0

Table 3: 40nm CMOS at TSMC Fab-14 Fab Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)	MIL-STD-883, M1015	125°C, 48 Hours	ADAU1787	Q13146.17	40	0
				Q13146.18	40	0
				Q13146.19	40	0
				Q13146.20	40	0
				Q13146.21	40	0
				Q13146.22	40	0
				Q13146.23	40	0
				Q13146.24	40	0
				Q13146.25	39	0
				Q13146.26	39	0
				Q13146.27	39	0
				Q13146.28	39	0
				Q13146.29	39	0
				Q13146.30	39	0
				Q13146.31	39	0
				Q13146.32	39	0
				Q13146.33	32	0
				Q13146.34	213	0
				Q13146.35	213	0
				Q13146.36	211	0
				Q13146.37	30	0
				Q13146.40	175	0
				Q13146.41	208	0
				Q13146.42	208	0
				Q13146.43	76	0
High Temperature Operating Life (HTOL)	JESD22-A108	125°C<Tj<135°C, Biased, 1,000 Hours	ADAU1860	Q17772.1.HO1	45	0
				Q17772.2.HO2	45	0
				Q17772.3.HO3	45	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	ADAU1860	Q17772.1.HS1	45	0
Temperature Humidity Bias (THB)[1]	JESD22-A101	85°C, 85%RH, Biased, 1,000 Hours	ADAU1787	Q13146.5	45	0
				Q13146.6	45	0
				Q13146.7	45	0
				Q15092.15	45	0
				Q15093.8	45	0
				Q16587.8	45	0

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM) and Field-Induced Charged Device Model (FICDM) ESD testing are summarized in Table 4. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link on Analog Devices' web site).

Table 4: ADAU1850 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	56-WLCSP	JS-002	1Ω, Cpkg	±1250V	NA	C3
HBM	56-WLCSP	ESDA/JEDEC JS-001	1.5kΩ, 100pF	±4000V	NA	3A

Latch-Up Test Results

Three samples of the ADAU1850 were latch-up tested at T_A=25°C per JEDEC Standard JESD78, Class I. All pins passed.

Passing Positive Current	Passing Negative Current	Passing Over-Voltage
+200mA	-200mA	1.8V, 2.7V

Approvals

Reliability Engineer: Arnold Naniong

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

TEST

PRODUCT

QUALIFICATION

REPORT

TITLE:

ADAU1850 Test Correlation Report for JC3 & UT1

PCN Number: 21_0236

REVISION: A

DATE: 14Dec, 2021

PROJECT BACKGROUND:

The ADAU1850 is currently undergoing production testing at the UT1(UTAC). It is a business strategic decision to qualify JC3(JCAP) to be additional test site to ensure continuity in supply. But for wafer fab and RDL process, they are all completed in TSMC and ship to UT1 and JC3 for probing test.

SUMMARY:

The ADAU1850 is a codec with three inputs and one output that incorporates one digital signal processor. The path from the analog input to the DSP core to the analog output is optimized for low latency and is ideal for noise canceling earphones. With the addition of a few passive components, the ADAU1850 provides a complete headset solution.

The ADAU1850 is a low power audio codec with an optimized audio processing core, making it ideal for noise canceling applications that require high quality audio, low power, small size, and low latency. The serial audio port is compatible with I2S, left justified, right justified, and time division multiplexing (TDM) modes, with tristating for interfacing to digital audio data. The operating voltage of AVDD and HPVDD is 1.8 V, and an internal regulator is used to generate the digital supply voltage.

The input signal path includes flexible configurations that can accept differential or single-ended analog microphone inputs. AIN2 supports single-ended analog microphone inputs only. Each input signal has its own programmable gain amplifier (PGA) for volume adjustment. The ADCs and DAC are high quality, 24-bit sigma-delta (Σ-Δ) converters that operate at a selectable 12 kHz to 768 kHz sampling rate and the ADCs also support 8 kHz or 16 kHz sampling rate in voice wake-up mode. The ADCs and DAC have an optional high-pass filter with a cutoff frequency of 1 Hz, 4 Hz, or 8 Hz and fine step digital soft volume controls.

The DAC output is capable of differentially driving a headphone earpiece speaker with 16 Ω impedance or higher. There is also the option to change to line output mode when the output is loaded differentially with ≥10 kΩ.

Test product transfer qualification was performed according to Analog Devices Specification to ensure two test sites are statistically equivalent. Same tester platform, test hardware is used in both sites, there is no change to the form, fit, function, quality and reliability of the product.

This report documents the successful completion of the product test transfer requirements for the release of ADAU1850 in JC3.

TEST AND PRODUCT INFORMATION:

Device: ADAU1850

Package: 0.4mm pitch, 2.957mm * 1.757mm WLCSP

Leads: 28 balls

Affected products:

Generics	FGs
ADAU1850	ADAU1850-W
	ADAU1850BCBZRL

Tester Platform: MFLEX-MS

Device Interface Board: P-69342 / P-75493

Test socket: P-71015

DESCRIPTION AND TEST RESULTS:

Below tables provide description of the qualification tests conducted and corresponding test results for ADAU1850. All the units have undergone electrical tests on both the sending and receiving sites on the same test platform. Any device that will not meet the electrical qualification requirements will mean failure of the qualification and require solid corrective actions and a repeat of the qualification process. Qualification activities performed, and acceptance criteria is shown on Table 1 below:

Table 1: *Qualification Activities and Acceptance Criteria*

Qualification Activity	Purpose	Sample Quantity	Accept Criteria
Device Repeatability Correlation	To check if the devices have stable performance from repeatability test and correlated for UT1 and JC3	4pcs units for each test site (Quad Sites Testing)	* Mean Shift ≤ 5% * CPK≥1.67 * Or other specified
Device Parametric Distribution Correlation	To check if the devices from UT1 and JC3 has the correlated parametric distribution for all tested items	100pcs units for each test site (Quad Sites Testing)	* Mean Shift ≤ 5% * CPK≥1.67 * Or other specified

Raw data and analysis report were analyzed and summarized in Table3 (Device Repeatability Correlation) and Table4(Device Parametric Distribution Correlation).

Table 2: *Lot Details for Correlation*

Device PN BACKEND SITE	FAB LOT# WAFER ID#	ASSEMBLY LOT#	DATE CODE
ADAU1850 **UT1**	P64188_#06	5521582.1	2146
ADAU1850 **JC3**	P64189_#07	5524512.1	2139

Table 3: *Device Repeatability Correlation Result*

Generic	Package	Lot Number	Repeatability Correlated between UT1 and JC3?
ADAU1850	28L -WLCSP	5521582.1(UT1)/5524512.1(JC3)	YES

Table 4: *Device Parametric Distribution Correlation Result*

Generic	Package	Lot Number	Parametric Distribution Correlated between UT1 and JC3?
ADAU1850	28L -WLCSP	5521582.1(UT1)/5524512.1(JC3)	YES

APPROVALS:

Technical Review Board No. TRB-65076- Add JC3 as new MP site for ADAU1850 WLCSP Testing

ADDITIONAL INFORMATION:

Homepage: https://www.analog.com/en/index.html

Product datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/adau1850.pdf

Customer Service: https://www.analog.com/en/support/technical-support.html

ADAU1850_Datasheet_Rev0 to Rev1_Specification_Comparison

Yellow denotes an increase or new index in specification

Data Sheet Rev.0 ADC2 Specifications

SINGLE-ENDED LINE INPUT	Typ	Unit
Total Harmonic Distortion Plus Noise (THD+N) (20 Hz to 20 kHz, −1 dB full-scale output)		
Enhanced performance	-78	dBFS
Normal performance	-78	dBFS
Power saving	-78	dBFS
Voice wake-up	-78	dBFS
SINGLE-ENDED PGA INPUT		
Total Harmonic Distortion + Noise		
Enhanced performance	-78	dBFS
Normal performance	-78	dBFS
Power saving	-78	dBFS
Voice wake-up	-78	dBFS

Data Sheet Rev.1 ADC2 Specifications

SINGLE-ENDED LINE INPUT	Typ	Unit
Total Harmonic Distortion Plus Noise (THD+N) (20 Hz to 20 kHz, −1 dB full-scale output)		
Enhanced performance	-81	dBFS
Normal performance	-81	dBFS
Power saving	-81	dBFS
Voice wake-up	-81	dBFS
SINGLE-ENDED PGA INPUT		
Total Harmonic Distortion + Noise		
Enhanced performance	-81	dBFS
Normal performance	-81	dBFS
Power saving	-81	dBFS
Voice wake-up	-81	dBFS

Datasheet Rev.1 Added RCOSC Specification

RCOSC	Test Conditions/Comments	Min	Typ	Max	Unit
Output frequency	After power on	21		30	MHz